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Implementation of 64-Bit ALU Using Modified Sqrt Carry Select Adder

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Abstract: In virtual pc, an Arithmetic Logic unit (ALU) is a powerful combinational circuit that executes arithmetic and logical capabilities. Parallel adder in ALU performs an critical function, however the deliver propagation (CP) takes maximum of the time for addition. For area-green packages, ALU the usage of modified Square Root Carry Select Adder (SQRT CSLA) is proposed and for higher speed packages, ALU the usage of modified SQRT CSLA via Carry Look Ahead (CLA) Adder is implemented. The paper gives you the design and implementation of 64-Bit ALU the usage of modified SQRT CSLA and binary extra counter. Compares it with the ALU the usage of everyday SQRT CSLA in terms of total number of simple gates. The design entry may be described in Verilog .For simulate and synthesize use Altera QUARTUS-II 9.1 .

INTRODUCTION:

The basic work is to use Binary to Excess-1 Converter (BEC) in the ordinary CSLA to acquire decrease location and expanded velocity of operation. This logic is changed in RCA with Cin=1. This logic can be implemented for distinctive bits which can be used inside the modified design. The most important gain of this BEC good judgment comes from the fact that it uses lesser quantity of common sense gates than the n-bit Full Adder (FA) shape. As said above the primary idea of this paintings is to apply BEC in preference to the RCA with Cin=1 in an effort to reduce the region and boom the rate of operation in the normal CSLA to obtain changed CSLA. To update the n-bit RCA, an n+1 bit BEC logic is needed. The shape and the feature table of a 6-bit BEC are shown in Figure1

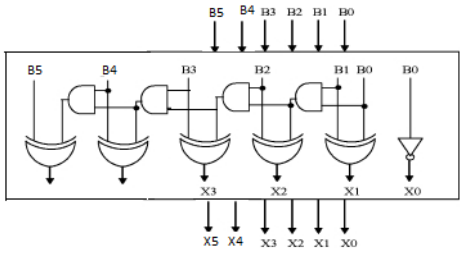

Figure 1: 6-binary to excess-1 converter

In designing virtual circuit, ALU performs an vital position in executing numerous mathematics and logic operations. Adder is

the primary unit for enforcing ALU. When computation for huge number of bits in ALU is needed, there's a want of cascading the adder circuit. These Cascaded adders however cause Carry Propagation Delay (CPD) thereby affecting the rate of operation. The delay in adder is prevailed via deliver to be propagated. Originally normal SQRT CSLA utilized Ripple Carry Adder (RCA)-RCA [1] configuration. Modified SQRT CSLA (MSC) utilized one RCA with Cin=0 and replaces the other RCA with Cin=1 by Binary to Excess-1 converter (BEC-1) [2]. In this paper 8-Bit, sixteen-Bit, 32-Bit and sixty four-Bit ALU is proposed using modified SQRT CSLA and also implemented ALU the usage of modified SQRT CSLA by CLA (RCA with Cin=0 replaces by way of CLA). ALU block [3], [4] does seven mathematics operations along side four logical operations as shown in determine 1. To carry out these operations, 3 pick strains (P [2], P [1] and P [0]) are used. Arithmetic Operations: Increment, Addition, Subtraction, Decrement, Transfer, Add with bring and Subtract with borrow. Logical Operations: AND, OR, XOR and Complement. To design an ALU, first designing of the segment that executes arithmetic operations is accomplished with out taking logical section into attention, then the logic expression from the mathematics circuit is realized and at ultimate modification is executed inside the arithmetic phase. Based on these design steps it's miles concluded that to perform each the operations bring propagation from one degree to the following degree want to be zero, at some stage in the logical operations. To achieve this, 0.33 selection input P [2] is ANDed with each deliver of adder. Regular SQRT CSLA incorporates of RCA (cascade of complete adders) Blocks, one with Cin=0 and different with Cin=1. This configuration removes the CPD through pre computing the addition for both cases (Cin=zero and Cin=1) of convey. Once the addition for both cases is computed, multiplexer acts as a spread unit that selects

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the sum as well as the deliver to be propagated to the following degree of the adder, in keeping with the deliver propagated from the previous adder level. The input with the aid of one. The input to BEC-1 is the output sum of RCA with Cin=0. Thus, it replaces RCA with Cin=1, thereby casting off RCA-RCA configuration in ordinary SQRT CSLA. BEC-1 makes use of one extra bit than the bits utilized by RCA. The multiplexer gets two inputs, one is from RCA with Cin=0 and different one from BEC-1 in step with the bit position after which selects the correct enter sign. The deliver from the preceding level adder acts as a manipulate signal of multiplexer unit. The common sense expressions for three-Bit BEC-1 are referred to underneath.

Q0 = ~R0

Q1=R0^R1

Q2=R2^ (R1&R0).

EXISTED METHOD

Regular SQRT CSLA [1] is reconstructed with ALU block is shown in figure 2. Each stage output convey of full adder in RCA Block is ANDed with P [2] (0.33 selection input). The output of AND gate (one input as previous degree bring and different as P [2]) acts as a variety input for each multiplexer unit. F [7:0] indicates the output characteristic of ALU.

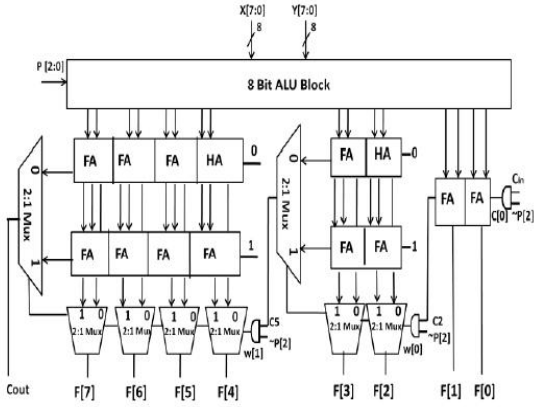

Figure2: 8-Bit ALU using Regular SQRT CSLA (RCA-RCA Configuration).

For low strength and vicinity-green packages [5], [7] the ALU is carried out the use of modified SQRT CSLA. Modified SQRT CSLA [2] is reconstructed with ALU block is proven in figure2

Figure3 eight-Bit ALU the usage of Modified SQRT

In modified ALU implementation, RCA with Cin=0 ends in CPD. It is located that the affect of this put off is decreased by using the usage of CLA as proven in parent 4. The advantage of the use of CLA is that the better order sum bit depends on enter deliver as opposed to intermediate carry. Output in adder should be available as quickly as the inputs are supplied but because of gates there's a finite put off in acquiring the output. As the quantity of bits is accelerated, consequently the number of stages will increase, consequently the transmission period for deliver to propagate increases. To avoid this dependency the deliver for every level is predicted by using CLA [6].

ARCHITECTURE OF PROPOSED MODIFIED 64-**BIT SQRT CSLA**

This structure is just like ordinary sixty four-bit SQRT CSLA, the best alternate is that, we replace RCA with Cin=1 a number of the two available RCAs in a group with a BEC. This BEC has a function that it could perform the same operation as that of the replaced RCA with Cin=1. Fig three shows the Modified block diagram of sixty four-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various agencies of variable sizes of bits with every institution having the ripple deliver adders, BEC and corresponding muxer . As shown inside the Fig.4, Group zero incorporate one RCA only that is having enter of lower sizeable bit and deliver in bit and produces result of sum[1:0] and perform that is performing as mux selection line for the following group, in addition the procedure continues for better corporations however they includes BEC logic in preference to RCA with Cin=1.Based on the attention of put off values, the advent time of selection input C1 of eight:three mux is in advance than the sum of RCA and BEC. For last organizations the selection enter arrival is later than the RCA and BEC. Thus, the sum1 and c1 (output from mux) are depending on mux and outcomes computed through RCA and BEC respectively. The sum2 relies upon on c1 and mux. For the ultimate parts the arrival time of mux choice enter is constantly greater than the arrival time of information inputs from the BEC's. Thus, the postpone of the remaining MUX relies upon on the advent time of mux choice input and the mux put off. In this Modified CSLA structure, the implementation code for Full Adder and Multiplexers of 6:three, eight:four, and 10:five up to 24:eleven were designed. The layout code for the BEC become designed by using the use of NOT, XOR and AND gates. Then 2, 3, 4, 5 as much as eleven-bit ripple deliver adder changed

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into designed.

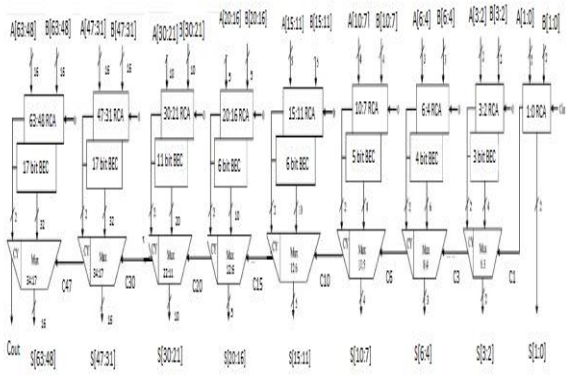

Figure4:Architecture of 64-Bit Modified SQRT CSLA

SIMULATION RESULTS

Flow Status	Successful - Mon Jun 19 17:17:34 2017
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	SQRTCSLA
Top-level Entity Name	sqrt_adder1
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	15 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	26 / 343 (8 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

Figure4:Design summary for 8 bit square root adder

Flow Status	Successful - Mon Jun 19 17:25:47 2017
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	SQRTCSLA
Top-level Entity Name	sqrt_adder2_64
Family	Stratix II
Met timing requirements	Yes
Logic utilization	1 %
Combinational ALUTs	140 / 12,480 (1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	194 / 343 (57 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

Figure5: Design summary for proposed 64 bit square root adder

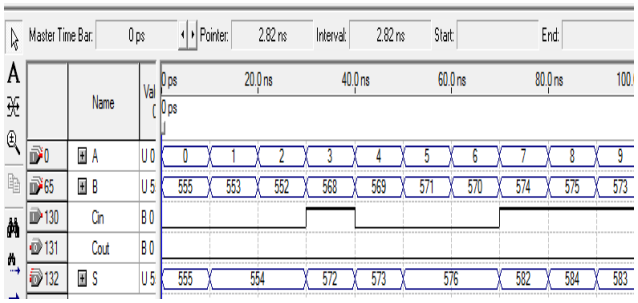

Figure5: Simulation results for proposed 64 bit square root adder

Flow Status	Successful - Mon Jun 19 17:29:39 2017
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	SQRTCSLA
Top-level Entity Name	alu4
Family	Stratix II
Met timing requirements	Yes
Logic utilization	4 %
Combinational ALUTs	354 / 12,480 (3 %)
Dedicated logic registers	64 / 12,480 (< 1 %)
Total registers	64
Total pins	198 / 343 (58 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	24 / 96 (25 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

Figure6: Design summary for proposed 64 bit ALU

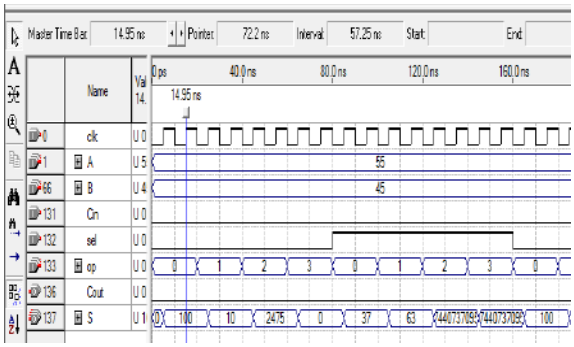

Figure7: Simulation Results for proposed 64 bit ALU

CONCLUSION

An efficient method is proposed in this paper to lessen the region and put off of SQRT CSLA architecture. The discount in the range of gates is acquired by means of simply replacing the RCA with BEC within the structure. The in comparison effects shows that the changed SQRT CSLA has a barely large place for lower order bits which further reduces for better order bits. The delay is reduced to a extremely good quantity with the changed SQRT CSLA. Thus the results suggests that using modified approach the place and delay will decrease as a consequence ends in proper opportunity for adder implementation for lots processors. The changed CSLA structure is therefore low location and excessive speed procedures for VLSI hardware implementation.The results obtrusive that 64 bit modified SQRT CSLA is used 354 combinational ALUs and 64 devoted registers.

The ALU layout and implementation using modified SQRT CSLA is for low strength and location-green programs. By introducing CSLA in ALU better overall performance is received in phrases of velocity. This paintings can be extended for the implementation of the 128-Bit ALU and there is a scope for VLSI application.

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