https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

Ultrasonic Signal Processing Using FPGA

A. Kushi[1], P. Suresh Babu[2]
[1]M.Tech Scholar, [2]Assistant Professor
[1, 2] Department of ECE, SVCE, Tirupati, India
Email: [1] kushi9700@gmail.com , [2] sureshbabu476@gmail.com,

Abstract*— *Ultrasonic nondestructive evaluation (NDE) has been widely used in quality assessment and failure analysis for critical structures. The NDE system is commonly designed on microcontrollers and digital signal processors, which fall short of meeting the demands of high speed and requirements of adaptability. This requires reconfigurable computing devices to implement the system. This study aims to build a prototype real time ultrasonic signal processing platform using Field Programmable Gate Array (FPGA). The platform acquires ultrasound data at the speed of 100 MSPS. The embedded system running on an FPGA is reprogrammable to evaluate signal processing algorithms and NDE methods. To demonstrate the system, a split spectrum processing algorithm is implemented and the result is displayed on a touch screen LCD. Thanks to the flexibility of FPGA, the platform is not limited to ultrasound NDE application. It may have a broader impact on future project development for signal processing research and education.

***Keywords*— FPGA, LCD, NDE, Touch Screen, Ultrasonic Signal Processing.**

I. INTRODUCTION

Ultrasonic nondestructive evaluation (NDE) has been widely used in quality assessment and failure analysis for critical structures or components in manufacturing, bridge structure, microelectronic packaging, and composite materials for aircraft structure [1-4]. The NDE system is commonly designed on microcontrollers and digital signal processors, which fall short of meeting the demands of high speed and requirements of adaptability. This requires reconfigurable computing devices to implement the system. FPGA is a semiconductor device which contains configurable logic blocks, programmable interconnects and flexible input/output blocks. It is widely used in applications of automotive, communications, industrial automation, motor control, video processing, and medical imaging fields. Without requiring hardware changes, the use of an FPGA expands the product life by updating data stream files. Additionally FPGAs have grown to have the capability to hold an entire system on a single chip.

This study aims to build a prototype ultrasonic signal processing platform using FPGA. The platform acquires ultrasound data at the speed of 100 MSPS. The embedded system running on an FPGA is reprogrammable to test new signal processing algorithms and new NDE standards/methods. To demonstrate the system, a split spectrum processing (SSP) algorithm is implemented and the result is displayed on a touch screen LCD. Thanks to the flexibility of FPGA, the platform is not limited to ultrasound NDE application. It may have a broader impact on future project development for signal processing research and education. Long term educational and research viability is one of goals. It means that new peripherals have to be interfaced with existing hardware without disrupting the operation of the system. Because of this it is crucial that the data acquisition system and signal processing be implemented on reconfigurable hardware (i.e., FPGA). A microcontroller or digital signal processor (DSP) might be able to meet the system specifications short term, but will not be viable in the long run as project or system requirements may be changed. The platform will enable implementation and testing of ultrasonic signal processing algorithms without the overhead of setting up the data acquisition aspect. It is practical to have real-time operation and detection with instantaneous results for ultrasonic NDE. The hardware and software components should be able to handle complex computations. The system can be modified from time to time to take the advantages of evolving research results such as new processing algorithms. Configurable hardware makes the system resilient to future changes. FPGAs can implement designs that would require many clock cycles to sequentially implement in a DSP or microcontroller, in very few cycles since they can create dedicated hardware to run a particular operation in a parallel way. Beyond this hardware designs can be adjusted without reprinting the circuit board. These qualities should be sufficient to justify that an FPGA is an efficient platform for high speed data acquisition and signal processing. FPGA can be programmed in hardware description language (HDL), which can produce a very efficient processing and computation design for a particular task. However it may take a longer

https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

implementation time when compared with higher level languages such as C language which is more versatile. By building an embedded system to the FPGA, high language tools such as C can be used together with HDL language. In this case, it becomes more important to perform hardware/software design partition. Using hardware and software in such a manner allows for great flexibility in system design. This flexibility in system level design is ideal since the proposed system is intended to perform versatile signal processing tasks. This paper is organized as follows: Section II briefly discusses the system platform. Section III discusses the system testing and results. Section IV concludes the paper.

II. ULTRASONIC SIGNAL PROCESSING PLATFORM

Generally speaking, three additional hardware components are needed for the ultrasonic signal processing platform. An analog to digital converter (ADC) is needed to acquire an ultrasonic signal for the system. A digital to analog converter (DAC) can send the processed signal out of the system. A touch screen display can also be interfaced with the system to view the data. A touch screen can be used to provide the user a method to change data acquisition or signal processing settings. The system level diagram is shown in Figure 1. It can be seen that,in term of interfacing, 3 controllers are needed for the system. The desired signal processing algorithm runs on the embedded system inside FPGA.

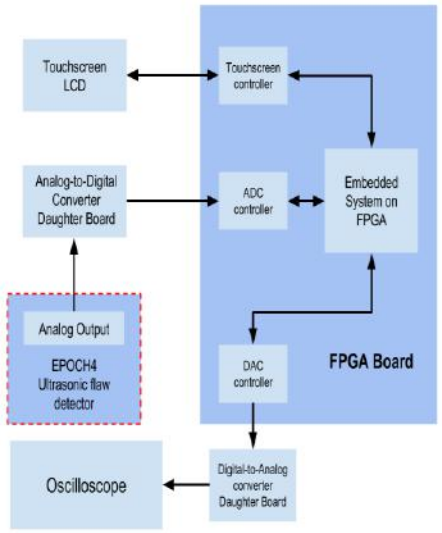

Fig-1: System level design for ultrasonic signal processing

Virtex-5 FPGA is chosen for capabilities to interface with the ADC, DAC, and ultrasonic equipment efficiently. It provides differential clock outputs, up to a 200 MHz system clock, differential and single ended general purpose input/output (GPIO) pins and RS-232 serial ports. The ADC chosen is the Maxim 1213N 12-bit ADC. It can operate at up to 170 MSPS. It has differential outputs, not single ended, which need to be accounted for when implementing the controller on the FPGA. The DAC chosen is the Maxim 5874 14-bit DAC. It has two analog outputs and two 14-bit input busses. It is chosen for compatibility with the other boards. The touchscreen device is the amulet STK-480272C which communicates with the FPGA over serial at 115200 baud. The ultrasonic device chose for the system is the EPOCH4 ultrasonic flaw detector. It provides the analog signal into the ADC and can be compared. Since the EPOCH4 can detect material defects and depth on its own the signal processing results of the platform can be compared with the EPOCH4 to verify their accuracy during testing. In full form the hardware specifications are listed follows. The Virtex 5 XC5VLX50T board interfaces with DAC and ADC peripherals, interfaces with the touch screen LCD board through UART, running under 100 MHz on-board system clock with 256 MB onboardDDR2memory and 32 MB flash memory. The MAX5874 EVKITDAC board provides 14-bit, high-dynamic performance in data conversion, and supports update rates of 200 MSPS. It operates under 3.3V and 1.8V supplies provided by the FPGA board and a MAX1536 voltage converter. It outputs a single ended analog signal between 0 and 2Vpp. The MAX1213N EVKIT ADC board provides12-bit low power data conversion, and supports a sampling rate up to 170 MSPS. It operates under 3.3V and 1.8V supplies provided by the FPGA board and a MAX1536 voltage converter. It accepts a single ended analog input signal between 0 and 2Vpp (EPOCH 4 ultrasonic flaw detector provides the analog signal source) and outputs 12 differential LVDS2.5 signals [5-6]. The Amulet STK 480272C LCD touch screen has serial port communication protocol with BAUD rate 115200 and provides 480x272 resolutions with refresh rate at 100 Hz [7]. Lastly, EPOCH4 ultrasound flaw detector, a standalone ultrasonic flaw detector, provides an analog reference to the system.

For the software design C will be used. The goals of the project need to be met by creating software that is modular. The reason for this is twofold so that the software can be updated easily as constraints change and so the platform can be used for a variety of applications in signal processing or communications just by changing the algorithm that processes the data. The software built for this design must be able to interface with the Microblaze

https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

embedded system and any addition hardware designs that are built to the system. Additionally software must directly control, or interface with a hardware controller, peripherals including the ADC, DAC, and touch screen daughter boards. In addition to the peripheral controllers a split spectrum processing algorithm is evaluated on the system [8-10]. The purpose of this algorithm is to be a placeholder for future signal processing algorithms that will be built to the system. This algorithm is a classic ultrasonic algorithm for target detection. It demonstrates typical signal processing characteristic for implementation on an embedded system, such as high speed timing constraints and parallelism in data processing. These characteristics help identify parameters needed for other algorithms to be implemented on the system. The implementation is done in C but needs to interface with dedicated hardware components for higher processing speed. The SSP algorithm diagram is shown in Figure 2.

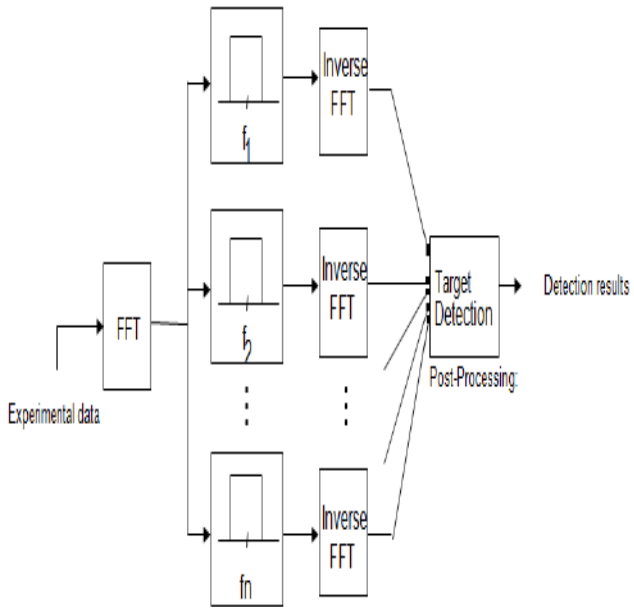

Fig-2: SSP algorithm

To implement the system on the FPGA, Xilinx Embedded development kit (EDK), software development kit (SDK), and Integrate software environment (ISE) Design Suite are used. ISE provides tools for implementation and simulation of VHDL. This allows us to create and implement hardware designs on the FPGA. Low level implementations like these are useful for high efficiency designs, but require more stringent knowledge of the system's hardware and do not make use of high level design tools. The EDK allows an embedded system to be built on the FPGA. Microblaze 32 bit soft-core RISC processor is used. VHDL designs may be imported as peripherals to the Microblaze processor on the FPGA. This gives good flexibility in how the system can be implemented. Many existing intellectual property (IP) cores provide complex, commonly used, or highly optimized functionality that can be added to the embedded system. On top of this implementation the SDK environment allows for C codes to be built to the Microblaze system. One such IP would be a hardware FFT. By using these tools in conjunction a developer has flexibility in how a system can be implemented to the FPGA. The embedded system running on the FPGA uses a 32-bit RISC 100MHzMicroblaze processor. It saves incoming data from ADC to the external DDR memory, and accepts the inputs from the GUI running on the touch screen board. The development environment, Xilinx embedded development kit (EDK) and software development kit (SDK), uses VHDL for the logic level hardware implementation of ADC and DAC

Controllers and C language for the drivers of ADC and DAC controllers, the interface of general purpose I/Os and UART, and signal processing algorithms. The ADC controller, implemented in VHDL, provides C APIs for the Microblaze processor. It accepts 12 differential LVDS2.5 inputs from the ADC board and forms a single-ended data vector for signal processing. The DAC controller, implemented in VHDL, provides C APIs for the DAC driver. It outputs a 14-bit data vector to the DAC board, operating at 100 MSPS. The touch screen controller, implemented in C language, outputs ASCII data to the touch screen board over RS232 and accepts inputs from the touch screen in ASCII format. The data structure is [*starting address in hex*] [*Upper nibble 1*] [*Lower nibble 1*] [*Upper nibble 2*] [*Lower nibble 2*] *… [Upper nibble N] [Lower nibble N] 0x00, where n*ibbles are in ASCII. For example, to send hex value 0x80, it sends 0x38 as the upper nibble and 0x30 as the lower nibble.

III. SYSTEM TESTING AND RESULTS

Various tests have been completed on the platform. The test of ADC controller: Data is being converted from the LVDS of the ADC by the differential signal input buffer instantiations within the VHDL to a single ended signal that can be processed by the FPGA. It requires LVDS_25 IO and differential termination resistors on GPIO pins to get the LVDS signals into the system properly. Output is being sent through in loopback between ADC and DAC and is observed to correlate properly. Figure 4 shows a test performed on the ADC to verify that the clock was being properly input into the ADC board. If the clock was not being received testing could not proceed since data

https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

would not be clocked into the system right. The top two differential signal forms a single-ended clock. In addition, Figure 5 shows the loopback testing of ADC and DAC. This result verifies that the ADC is outputting the data correctly. There is some phase difference, but the signals are very close in amplitude and frequency. Figure 6 is a test performed to establish a range of frequencies the ADC would work over.

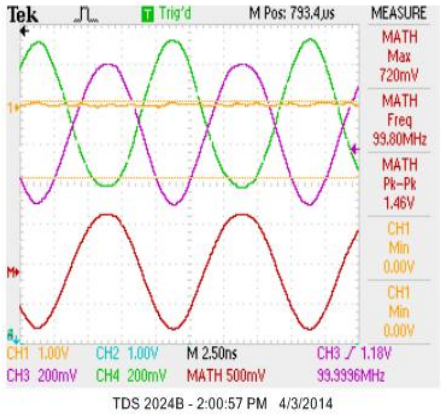

Fig-4: LVDS clock outputs from ADC. Top: differential clock signals Bottom: single-ended clock signal

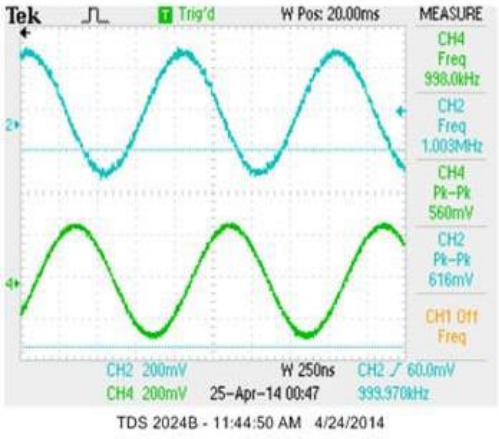

Fig-5: Loopback test of ADC and DAC. Top: the input to the ADC device, Bottom: the output of DAC device

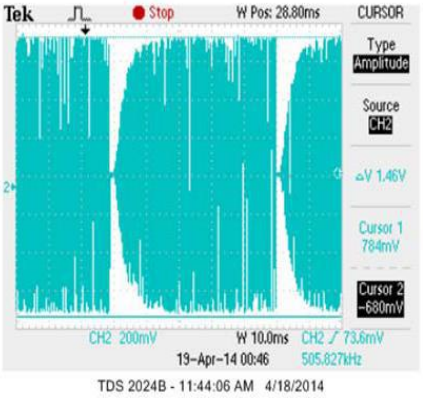

Fig-6: Loopback of a chirp from 10 kHz to 10 MHz

A SSP processing algorithm has been implemented in C. The algorithm was tested in Mat Lab then implemented in SDK in C. The algorithm works properly, but takes upwards of 50 seconds to complete. Currently the system is simply too slow to interface with the system at the rate data is being sampled. It would be ideal to switch some aspects of the function, especially the FFT and minima detection to hardware processes in VHDL. The issue comes from floating point operations. Switching to fixed point logic would speed the process up, but it would be easier to use an existing FFT IP core and get an even larger boost of speed than moving the function to fixed point. Post processing of the filter banks could also be done in parallel in hardware to speed up the system. This type of acceleration is addressed in [9-10]. Here the SSP algorithm is mainly utilized to validate the proto type system. Figure 7 shows the raw ultrasonic data. Figure 8 and 9 show the results of SSP algorithm using MATLAB and the FPGA implementation respectively.

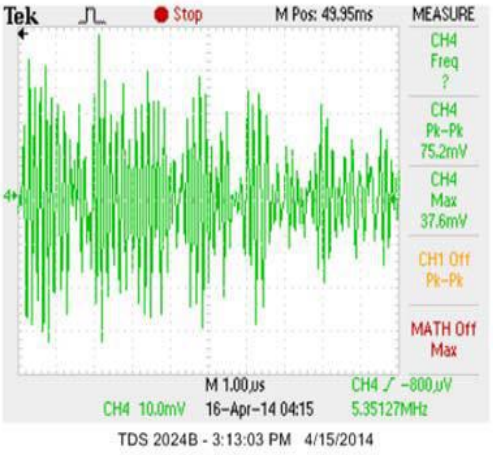

Fig-7: Raw Ultrasonic Signal

https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

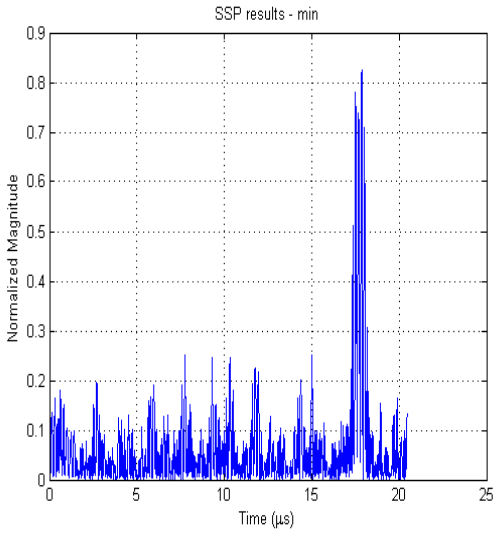

Fig-8: MATLAB result of SSP algorithm

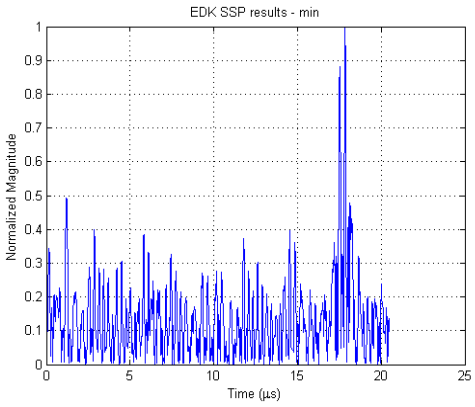

Fig-9: FPGA implementation result of SSP algorithm

A touch screen controller has been successfully implemented in C in the SDK. The user interface for the touch screen was designed with Amulet's touch screen interface design software GEM studio. The interface has buttons that can be used for future functionality, such as scaling the data set on screen. The touch screen can receive and plot any ultrasonic data sent from the FPGA. The FPGA can also receive touch screen inputs and respond to them. The serial code has been implemented using the Uartlite IP core in the EDK. The related result is shown in Figure-10.

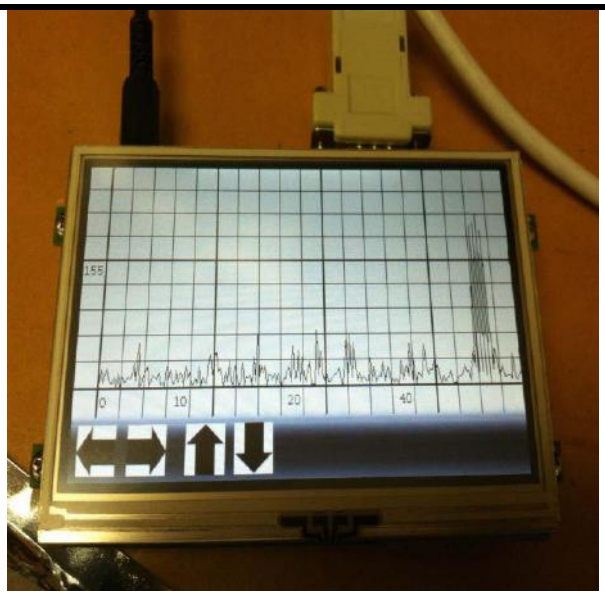

Fig-10: Signal detection displayed on Amulet Touch screen.

IV. CONCLUSION

In this study, an FPGA-based ultrasonic signal processing platform has been developed. ADC and DAC controllers have been implemented in hardware to interface high speed ADC and DAC daughter boards. In addition, a touch screen controllers have been implemented on the embedded system in C and communicate the touch screen device over RS232 serial port. The SSP algorithm has been evaluated on the embedded system in C. Overall the system components have been made but further work needs to be done to further tune the system for different applications. It may have a broader impact on future project development for signal processing research.

Scope for future work

The scope for further improvement, the following suggestions may prove useful for future work:

REFERENCES

[1] H. Choi and J. S. Popovics, "NDE application of ultrasonic tomography to a full-scale concrete structure," in *IEEE Transactions on Ultrasonics,Ferroelectrics, and Frequency Control*, vol. 62, no. 6, pp. 1076-1085, June 2015.doi: 10.1109/TUFFC.2014.006962

[2] H. M. La, N. Gucunski, Seong-HoonKee, J. Yi, T.Senlet and Luan Nguyen, "Autonomous robotic

https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

system for bridge deck data collection and analysis," *Intelligent Robots and Systems (IROS 2014), 2014IEEE/RSJ International Conference on*, Chicago, IL, 2014, pp. 1950-1955. doi: 10.1109/IROS.2014.6942821

[3] TribikramKundu, Ultrasonic and Electromagnetic NDE for Structure and Material Characterization: Engineering and Biomedical Applications, ISBN: 9781439836637, CRC press, June 2012.

[4] I. Pelivanov, A. Shtokolov, Chen-wei Wei and M. O'Donnell, "A 1 kHz a-scan rate pump-probe laser-ultrasound system for robust inspection of composites," in *IEEE Transactions on Ultrasonics, Ferroelectrics, andFrequency Control*, vol. 62, no. 9, pp. 1696-1703, Sept. 2015. doi: 10.1109/TUFFC.2015.007110

[5] Maxim Integrated, Inc., MAX5873/MAX5874/MAX5875 Evaluation Kits board manual, 2006. https://datasheets.maximintegrated.com/en/ds/MAX5873EVKITMAX5875EVKIT.pdf

[6] Maxim Integrated, Inc., MAX1213N/MAX1214N Evaluation Kits board manual, 2006. https://datasheets.maximintegrated.com/en/ds/MAX1213NEVKIT.pdf

[7] Amulet Technologies, Amulet STK-480272C manual, 2012.

[8] E. Oruklu, and J. Saniie,"Hardware efficient realization of a real time ultrasonic target detection system," *IEEE Transaction on Ultrasonics,Ferroelectrics, and Frequency Control*, vol. 56, no. 6, pp. 1262-1269, June 2009.

[9] H. C. Sun, and J. Saniie, "Ultrasonic flaw detection using split-spectrum processing combined with adaptive network based fuzzy inference system," *IEEE Proceedings of Ultrasonic Symposium*, vol.1, pp. 801- 804, 1999.

[10] J. Saniie, E. Oruklu and S. Yoon, "System-on-chip design for ultrasonic target detection using split-spectrum processing and neural networks," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and FrequencyControl*, vol. 59, no. 7, pp. 1354-1368, July 2012. doi:10.1109/TUFFC.2012.2336