Trends in Engineering and Technology (NCTET-2K17)
International Journal of Advanced Engineering Research and Science (IJAERS) *Special Issue-4*
https://dx.doi.org/10.22161/ijaers/nctet.2017.ece.22 *ISSN: 2349-6495(P) | 2456-1908(O)*

ECG Data Acquisition System with 0.5v supply by using digital front end architecture

G CHANDRA SEKHAR[1], Dr. C CHANDRA SEKHAR[2]
[1]PG Scholar, Dept of ECE(VLSI Design),S.V.college of engineering,Tirupathi , India.E-mail:chandracharan239@gmail.com
[2]Professor & HOD, Dept of ECE, S.V.engineering college for womens, Tirupathi, India, E-mail: hod_ece@svew.edu.in

Abstract: Due to the popularity of portable electronic products, low power system has attracted more attention in recent years. Dynamic power consumption remains to be the biggest contributor to the total power consumption of a hardware design. One of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, which is responsible for thirty to seventy percentage of the total dynamic power consumption .A new power efficient electrocardiogram acquisition system that uses a fully digital architecture to reduce the power consumption and chip area. A design of analog-to-digital converters (ADCs) based on digital delay lines. Instead of analog block, they convert the input voltage into a digital code by delay lines and are mainly built on digital blocks .The proposed architecture is a moving average to voltage to time converter is used. The circuit implemented in 0.18um CMOS technology. The simulation results shows that the front end of the circuit consumes 274 nW of power.

Keywords: Digital Integrated Circuit (IC), Electrocardiogram (ECG), Low Power, Moving Average Filtering, Offset Cancellation.

I. INTRODUCTION

Biomedical devices are becoming more popular. This is due to the rapid advancement of integrated circuit (IC) fabrication. Such devices are being used as wearable or implantable gadgets as well as monitoring equipment. In all these applications, the biosignal is first preconditioned and converted to digital. A digital signal processor then processes the digital data for monitoring or diagnosis applications. Biomedical signal acquisition systems typically consist of a low-noise amplifier (LNA) , a bandpass filter, an analog sample-and-hold, and an analog-to-digital converter (ADC), as shown . While the architecture shown is typically used, in some cases chopping technique is used to reduce the impact of the flicker noise, as shown .With the advancement of CMOS technology, the supply voltage is being reduced, which decreases the voltage headroom for analog block of an IC. Although the technology scaling leads to lower power consumption and higher performance in digital circuits; many parameters [such as signal-to-noise ratio (SNR), dynamic range, gain, and so on] of the analog parts of an IC are negatively impacted. Therefore, it is desirable to find new architectures, in which more digital blocks are used. Recently, a few methods, which are based on digital techniques, are introduced.

The block diagram of the system designed. In this circuit, many of the functions that are typically implemented by analog blocks are performed by digital circuits. Using this digitally enhanced approach can help increase the flexibility of the system in removing unwanted interferences. Moreover, digital calibration techniques can be used more easily. Eliminating the interferences at the input of the system, before substantial gain is applied, can relax the dynamic range requirements and minimize the supply voltage. This can lead to reduce the overall power consumption and area; both of which are critical for implantable and multi-electrode systems .This is achieved using mixed signal feedback and digital block. Hence, it appears that the use of digital techniques in the implementation of these systems can lead to a better performance and better compatibility with digital CMOS technology. However, there are other issues that should be addressed before moving toward fully digital implementation. Two of these issues are as follows.

- Removing the DC Offset Voltage of Electrodes Without Passive Elements: In these systems, a dc offset voltage as large as 50 mV is associated with the electrodes. Typically this offset is removed by ac coupling the instrumentation amplifier with the electrode. This is not very desirable, since it requires large capacitors.
- Providing a Solution for Antialiasing Filter: Antialiasing is typically done by low-pass analog filters. Box car samplingtechnique can be a solution for the fully digital implementation .Motivated by the above-mentioned issues, we have designed a new fully digital electrocardiogram (ECG) signal acquisition system. The circuit is designed in0.18-um CMOS technology and operates by a supply voltage of 0.5 V.

An electrocardiogram (ECG) is a recording of the electrical activity on the body surface generated by the heart. ECG measurement information is collected by skin electrodes placed at designated locations on the body. The ECG signal is characterized by six peaks and valleys labeled with successive letters of the alphabet P, Q, R, S, T, and U in Fig.1.This article suggests some ideas for a low-cost implementation of an ECG monitor.Its configuration is envisaged for use with a personal computer (PC). Although this article is written with patient

safety in mind, any ideas presented are not by themselves necessarily compatible with all system safety requirements; anyone using these ideas must ensure that, in a particular design, the design as a whole meets required safety criteria.

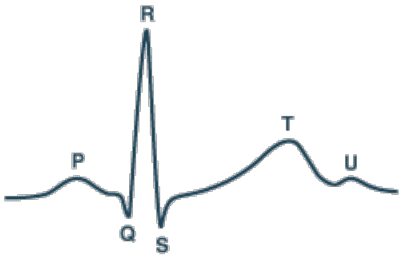


Fig.1. ECG signal.

II. PROPOSED FULLY DIGITAL FRONT END ARCHITECTURE

Fig.2 shows the block diagram of the proposed fully digital architecture. In this structure, the processing of the biosignal is performed in the time and digital domain. Hence, the advantages of digital CMOS technology are utilized. The analog biosignal coming from the electrode is directly connected to the front-end circuit and is converted to time with a voltage-to-time converter (VTC). From this point on in the circuit, the signal information is in the phase of the VTC output signal. The output of the VTC is applied to the time-mode processing block, in which the antialiasing and offset cancellation are done in time domain. Then, a time-to-digital converter (TDC) transfers the time-mode signal into digital domain where other processes (digital filtering data compression / reduction , and so on) are performed.

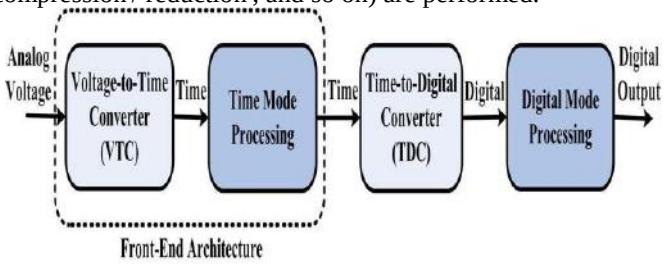


Fig.2. Overall block diagram of the proposed system.

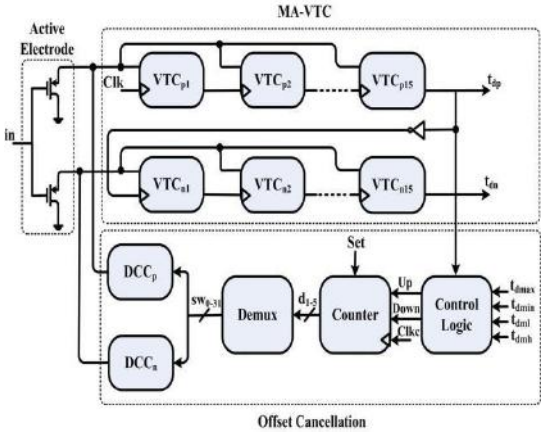


Fig.3. Proposed digital front-end architecture.

The proposed digital architecture is shown in Fig.2. It consists of an active electrode, two digital-to-current converters (DCCs), a moving average VTC (MA-VTC), a control logic block, a counter, and a demultiplexer In this architecture ,ac coupling capacitors are removed, and the impact of the electrode offset on the circuit is cancelled via a feedback loop. The technique used for the offset cancellation. As explained earlier inconventional biosignal acquisition systems, an LNA is used after the electrode. In the proposed architecture, this block is removed. In the following text, each of the blocks of the proposed architecture is shown in Fig.3 is explained.

A. Active Electrode

An active electrode is an electrode, in which some active elements are used to reduce the power line interference .Two different two-wired active electrodes for comparison.

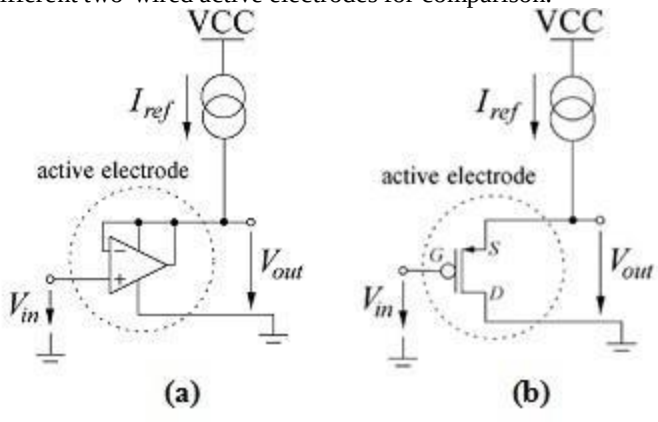


Fig.4. Active electrode with either (a) an op-amp or (b) a MOS transistor, both operating as a voltage follower.

The circuit uses an op-amp, while the one is implemented using a single transistor in Fig.4. Important parameters of such electrodes, such as offset, noise, gain, and output resistance, are compared .It has a superior performance in terms of noise, common mode rejection ratio (CMRR), and power consumption compared with the circuit .However, the offset and the output resistance are worse. Since, in ECG applications, the most important limiting factor is the input noise of the system, we have used the active electrode with a single MOS transistor in shown in Fig.4. An electrode in an electrochemical cell is referred to as either an anode or a cathode (words that were coined by William Whewell at Faraday's request). The anode is now defined as the electrode at which electrons leave the cell and oxidation occurs, and the cathode as the electrode at which electrons enter the cell and reduction occurs. Each electrode may become either the anode or the cathode depending on the direction of current through the cell. A bipolar electrode is an electrode that functions as the anode of one cell and the cathode of another cell. A primary cell is a special type of electrochemical cell in which the reaction cannot be reversed, and the identities of the anode and cathode are therefore fixed. The anode is always the negative electrode. The cell can be discharged but not recharged.

A secondary cell, for example a rechargeable battery, is a cell in which the chemical reactions are reversible. When the cell is being charged, the anode becomes the positive (+) a the

cathode the negative (−) electrode. This is also the case in an electrolytic cell. When the cell is being discharged, it behaves like a primary cell, with the anode as the negative and the cathode as the positive electrode. In a vacuum tube or a semiconductor having polarity (diodes, electrolytic capacitors) the anode is the positive (+) electrode and the cathode the negative (−). The electrons enter the device through the cathode and exit the device through the anode. Many devices have other electrodes to control operation, e.g., base, gate, control grid.

B. Voltage To Time Converter (VTC)

In the proposed digital implementation, the analog input voltage is converted to a measurable time via a VTC at the first stage. The signal information is now in the delay of the clock signal (CLK). We have used both the positive and the negative VTCs in our design to implement a moving average filter (as will be explained later). The cascaded stages of VTCs form delay-line structures. A major advantage of the delay-line-based structure lies in its all-digital implementation. In addition, the delay line structure introduces time-domain amplification into the design. In particular, the input signal can be amplified in the time domain by simply extending the time window (using more VTC stages). This is in contrast to voltage amplification involving complicated analog amplifiers in the conventional systems. A straightforward way is the voltage-to-time-to-digital approach is shown in Fig.5. The sampled input voltage Vin is first converted to a time window T(Vin), which is then quantized by TDCs. This design stems from integrating ADCs, which are believed to be suitable for high-resolution applications.

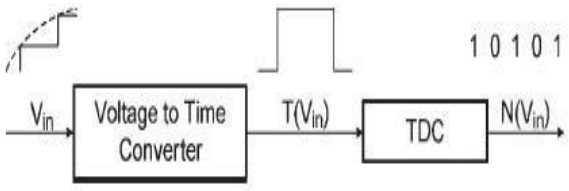


Fig.5.Illustration of voltage-to-time-to-digital ADCs.

C. Moving Average Filtering

Since, VTCs work with a clock and are broadband compared with the signal bandwidth, not using an antialiasing filter before VTCs would lead to out-of-band noise aliasing. To prevent aliasing and to avoid having an analog filter in the design, we have developed the structure shown in Fig.6 for converting the voltage-to-time as well as antialiasing filtering.

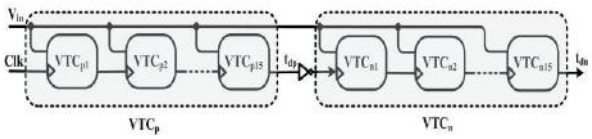


Fig.6. Schematic of the MA-VTC circuit.

The VTC should be designed in such a way that the small amplitude of the input voltage generates a large enough delay, linearly. In order to have time-domain amplification and acceptable SNR it can be shown in Fig.6, we have used 15 stages of positive VTC (VTC_p) and 15 stages of negative VTC (VTC_n).

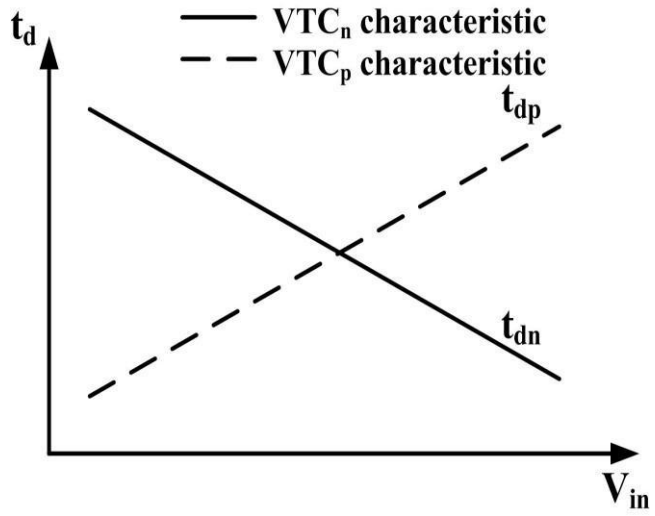


Fig.7.VTCn and VTCp characteristics.

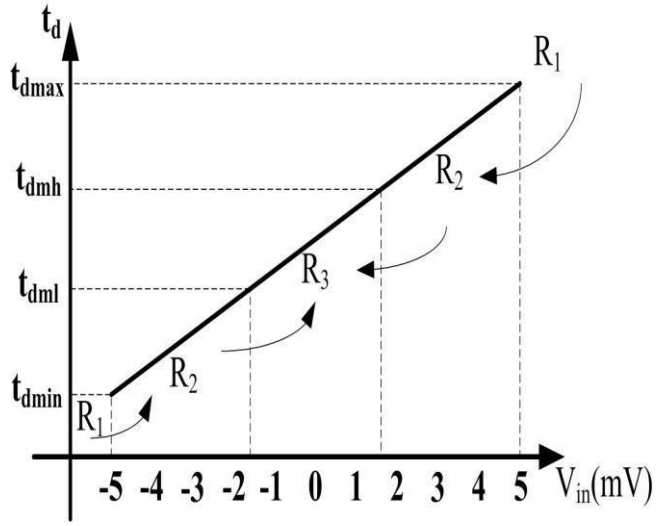


Fig.8. Characteristic of the VTCp in the ±5-mV range.

The delays versus input voltage of VTC_p and VTC_n are shown in Fig.7. As the input voltage becomes larger, the delay of VTC_p increases, while the delay of VTC_n decreases. In Fig.8 shows the characteristic of VTC_p. The VTC is linear in the range of −5 to +5 mV. This linear region is divided into two regions of R_2 and R_3. R_2 is related to the region for which $t_{dmh} < t_d < t_{dmax}$ or $t_{dmin} < td < t_{dml}$. Similarly, R3 shows the region for which tdml $< td < t_{dmh}$. Besides R2 and R3 regions, R_1 represents regions, in which the input is out of predefined linear range, ±5 mV, of the VTC (i.e., the delay is more than t_{dmax} or less than t_{dmin}). Assuming that the maximum amplitude of the input signal is ±2.5 mV, the delay goes in the R_1 region if the value of the offset exceeds ±2.5 mV. This happens for all the VTCs in the chain. The sum of these integration periods is equal to the clock period. Hence, the integration over this time window can be represented by

$$Y(T_s,t) = \frac{1}{T_s}\int_{t-T_s}^{t} V_{in}(\tau)\, d\tau \quad (1)$$

Therefore, its impulse response is a rectangular pulse in the range of [0, Ts].

$$h(t) = \frac{1}{T_s}\int_{t-T_s}^{t} \delta(\tau)\, d\tau = u(t) - u(t-T_s) \quad (2)$$

Hence, its frequency response is a sinc function

$$H(jw) = \frac{2\sin\left(\left(\frac{T_s}{2}\right)\omega\right)}{\omega T_s} \quad (3)$$

In this way, the moving average filtering is embedded in the MA-VTC, preventing aliasing of the wideband noise.

D. Clock Frequency And Signal Recovery

VTC_p and VTC_n blocks are designed in such a way that the absolute slopes of their characteristic curves are equal. Hence, for any input voltage, we can write

$$t_{dp} + t_{dn} = t_{tot} = Constant \quad (4)$$

The delay time t_{dp} (or t_{dn}) of a VTC gate is supposed to be a linear function of its input voltage and is given by

$$t_{dp} = \alpha V_{inp} + \beta_1 \quad (5)$$

$$t_{dn} = -\alpha V_{inn} + \beta_2 \quad (6)$$

where V_{inp} and V_{inn} are the input voltage during the time interval that the clock pulse passes through VTC_p and VTC_n, respectively. In addition, α and β1,2 are constants. The clock period, T_{clk}, must be chosen such that for the maximum variation of the input t_{dn} is not zero and is always measurable. Therefore, the clock period should be slightly more than t_{tot}. Hence

$$T_{clk} \geq t_{dp} + t_{dn} = \alpha\left(V_{inp} - V_{inn}\right) + \beta_1 + \beta_2 \quad (7)$$

The outputs of the digital front end are t_{dP} and t_{dn}. These delays are converted to two digital numbers (DP and DN)by two TDCs. The digital number corresponding to the input voltage, Din, can be obtained from

$$D_{in} = \frac{D_p - D_n}{2D_\alpha} + \frac{D_{\beta 2} - D_{\beta 1}}{2D_\alpha} \quad (8)$$

where D_α, $D_{\beta 1}$, and $D_{\beta 2}$ are digital numbers of α, β_1, and β_2, respectively.

III. PROPOSED OFFSET CANCELLATION TECHNIQUE

The ECG signal acquisition system should be capable of rejecting the dc polarization voltage of the biopotential electrodes, appearing as a dc offset at the input. This requires a high-pass filter (HPF) with a cutoff frequency <1 Hz. This filter requires large capacitors and on-chip implementation of such a filter is not efficient in terms of area. In the proposed architecture, a new offset cancellation technique is used, in which offset cancellation is done in two stages.

A. Algorithm

Large amounts of electrode offset make the MA-VTC circuit nonlinear and saturated, to avoid this; we designed MA-VTC circuit, such that it is linear for twice the maximum ECG signal amplitude. The impact of the offset is cancelled by the following algorithm. Fig. 8 shows the characteristic of VTC_p. The VTC is linear in the range of −5 to +5 mV. This linearregion is divided into two regions of R_2 and R_3. R_2 is related to the region for which $t_{dmh} < t_d < t_{dmax}$ or $t_{dmin} < t_d < t_{dml}$. Similarly, R_3 shows the region for which $t_{dml} < t_d < t_{dmh}$. Besides R_2 and R_3 regions, R1 represents regions, in which the input is out of predefined linear range, ±5 mV, of the VTC(i.e., the delay is more than t_{dmax} or less than t_{dmin}). Assuming that the maximum amplitude of the input signal is ±2.5 mV, the delay goes in the R_1 region if the value of the offset exceeds ±2.5 mV. In this case, due to the offset, the circuit behaves nonlinear and may be saturated. When the input falls in the R1 region, offset cancellation block distinguishes this by comparing td with t_{dmax}/t_{dmin}, and reduces the offset, such that the circuit goes back in R_3. The DCC block [Fig. 3(b)] is in the charge of this shift of the operation region. With reducing the offset and putting the circuit in the R_3 region, the operation remains linear. The R_2 region is considered in order to add a hysteresis to the system so that the offset cancellation block does not activate very frequently.

B. Architecture

The block diagram of the proposed offset cancellation technique is shown in Fig. 9. It contains two 5-bit DCCs, control logic circuit, 5-bit counter, and 5–32 demultiplexer (Demux). Since the offset voltage changes very slowly, the frequency of the clock signal used for the counter (C_{lkc}) is ∼10 times less than the clock of the rest of the circuit. In this structure, the output delay of the VTC_p block, t_{dp}, is compared with t_{dmax} and t_{dmin} in the control logic block by a time comparator (TC) to determine the operation region of the VTC_p (i.e., R_1, R_2, or R_3). If the delay is more (less) than t_{dmax} (t_{dmin}), the DOWN (UP) signal will be set by the control logic block. The output of the counter changes accordingly and is applied to the D_{emux}, which controls the DCC. The DCC generates a current proportional to its digital input anddecreases/increases the input voltage of the VTC_p and VTC_n,

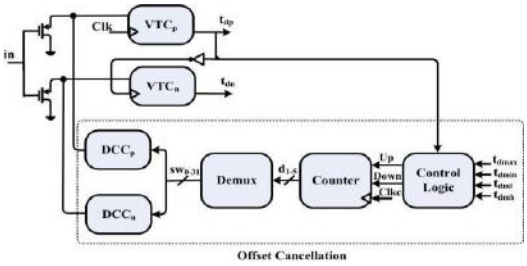
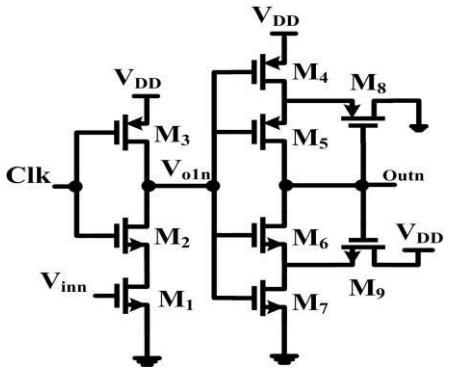
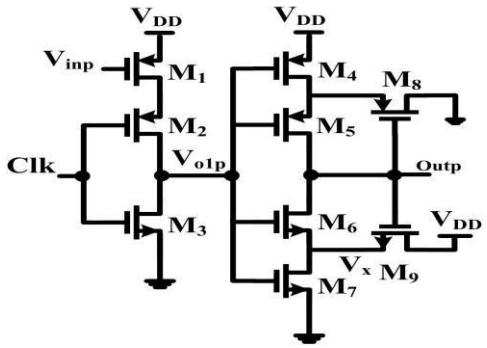


Fig.9. Proposed offset cancellation block diagram

Process variations can shift the delay to region R1. The digital feedback loop brings back the delay to region R3 and the impact of the process variations is cancelled.



(a)



(b)

Fig.10. VTC circuit. (a) Controlled by a pMOS transistor used in VTC_p blocks. (b) Controlled by a nMOS transistor used in VTC_n blocks.

The above-mentioned algorithm has the advantage of cancelling the impact of process variations. Process variations can shift the delay to region R1. The digital feedback loop brings back the delay to region R3 and the impact of the process variations is cancelled as shown in Fig.10.

IV. CIRCUIT DESIGN

The proposed fully digital front end is implemented in the 0.18-um CMOS technology to evaluate its performance. The supply voltage is 0.5 V, and the circuits are designed to operate in the subthreshold region to reduce the power consumption. Each block of the system and its design challenges is discussed in the following sections.

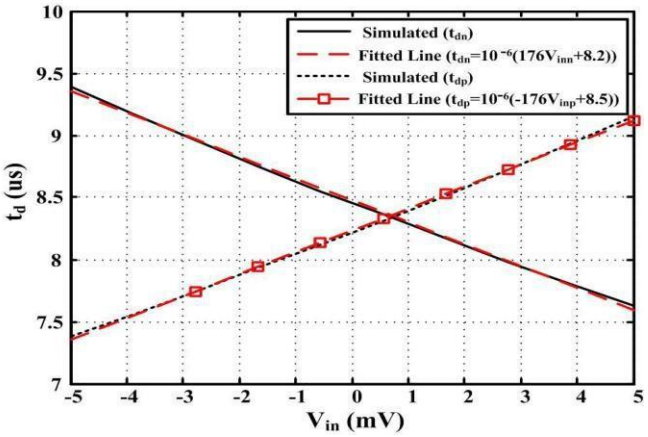


Fig.11. Delay of the voltage to time converter from simulation and the line fitted to the simulation data, for VTC_p and VTC_n circuits.

A. VTC Circuit

Fig11 shows the circuits of the VTCs used in VTC_p and VTC_n blocks (each block contains 15 stages of these cells). It consists of a current-starved (CS) inverter and an inverting Schmitt trigger. As can be seen in this figure, the input voltages, V_{inp} and V_{inn}, control the current passing through transistor M1 and change the rise/fall delay of the CS inverter. The Schmitt trigger circuit at the output of the CS inverter is used to sharpen the rising/falling edge of the clock at the output. This helps reduce the jitter and power consumption in the succeeding stages. Fig. 11 shows the characteristic curve of the VTC_n and VTC_p at the typical process corner (TT). The clock frequency in this simulation is 57.8 kHz. As can be seen, the delay changes almost linearly with the input voltage of the VTC. The dashed line in this figure shows the line fitted to the simulation data.

B. Control Logic

The control logic diagram is shown in Fig.12. It is composed of of TCs, AND and OR gates, and set-reset (SR) latches. For detecting the offset, the control logic should compare t_{dp} with four predefined delays (t_{dmax}, t_{dmin}, t_{dml}, and t_{dmh}).

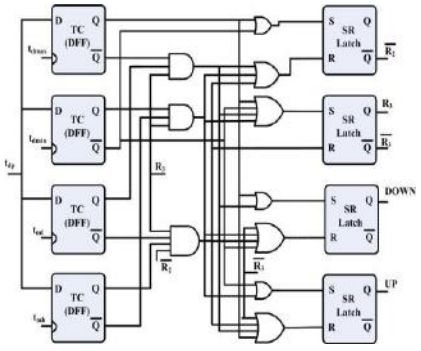


Fig.12. Schematic of the control logic.

The control logic diagram is shown in Fig.12. It is composed of TCs, AND and OR gates, and set-reset (SR) latches. For detecting the offset, the control logic should compare t_{dp} with four predefined delays (t_{dmax}, t_{dmin}, t_{dml}, and t_{dmh}). Note that in an analog front end, for detecting the offset voltage, an analog voltage comparator should be used. In our design, the offset is detected by TCs, which are implemented by D flip-flops and are more power and area efficient compared with the analog voltage comparators. The outputs of the control logic circuit are the UP and DOWN signals, which control the up/down counter in the offset cancellation block.

C. Counter

A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely-used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of largerintegratedcircuits.

D. DCCS Circuit

In the fully digital ECG front-end architecture of two DCC blocks are used. These blocks are in charge of generating a current that depends on the 32-bit digital number (SW0 to SW31) at the output of the Demux. The DCC circuit is in which the lower circuit generates the gate voltages required for the reference current generator in the upper circuit. The currents produced by transistors M_{0p} toM_{32p} and M_{0n} to M_{32n} pass through transistors M_p and M_n to generate the two voltages V_{inp} and V_{inn}. These voltages are then applied to the VTCp and VTC_n blocks as shown in Fig.13

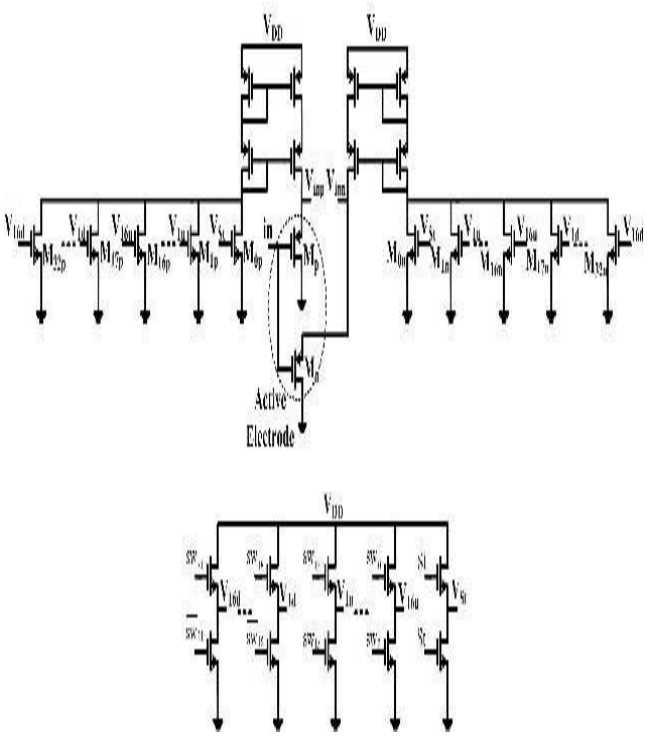


Fig.13. Structure of the current DCCs.

V. SIMULATION RESULTS

The proposed architecture is implemented in 0.18-um CMOS technology. The offset cancellation mechanism brought back to the operating region R3.The circuit operate in region R3 and moves to region R2 as the offset of input increases .when the input voltage reaches 11mv,the offset cancellation circuit detects this shift cancels the impact of the input offset. After recovery ,the whole signal is present in the output digital signal and digital filtering should be done finally. The power consumption of the overall front end is274 nW and is noticeably less than other mixed-signal ECG front-end circuits. This can be considered as one of the main advantages of the proposed fully digital architecture.

VI. CONCLUSION

In the expectation of the future dominance of digital CMOS technology, we have implemented a fully digital front-end architecture for an ECG acquisition system. In this system, passive elements, LNA, and analog filters are not used. The proposed digital architecture is compact and power efficient compared with the other analog implementations of these systems. A moving average mechanism embedded into the VTC of the front end eliminates the need for antialiasing filter. The proposed architecture is simulated in 0.18-um CMOS technology at 0.5 V supply voltage. The simulated power consumption is 274 nW.

VII. REFERENCES

[1]X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," IEEE J. Solid-State Circuits, vol. 44, no. 4, pp. 1067–1077, Apr. 2009.

[2]R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," IEEE J. Solid-State Circuits, vol. 38,no. 6, pp. 958–965, Jun. 2003.

[3]H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad, and A. M. Sodagar, "Analysis and design of tunable amplifiers for implantable neural recording applications," IEEE J. Emerg. Sel. Topics Circuits Syst, vol. 1, no. 4, pp. 546–556, Dec. 2011.

[4]M. S. J. Steyaert and W. M. C. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," IEEE J. Solid-State Circuits, vol. 22, no. 6, pp. 1163–1168, Dec. 1987.

[5]W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," IEEE Trans. Biomed. Circuits Syst., vol. 1, no. 2, pp. 136–147,Jun. 2007.

[6]T. Denison, K. Consoer, A. Kelly, A. Hachenburg, and W. Santa,"A 2.2 μW 94 nV/√Hz, chopper-stabilized instrumentation amplifier for EEG detection in chronic implants," in IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers (ISSCC), 2007, pp. 162–594.